LISTING OF CLAIMS

1. (Currently Amended) An electronic component, comprising:

an integrated circuit embodied on a monolithic substrate and incorporating:

a tuning module of the direct sampling type configured to receive ~~that receives~~ satellite digital television analog signals composed of several channels; and

several channel decoding digital modules connected at an output of the tuning module so as to deliver respectively and simultaneously several streams of data packets corresponding to several different selected channels.

2. (Currently Amended) The component according to Claim 1, wherein the channels extend over a predetermined frequency span and the analog signals convey digital information coded by digital modulation, and

wherein the tuning module comprises:

an analog stage receiving the said analog signals;

a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the frequency span; and

several digital devices for transposing frequencies that are connected to the output of the analog conversion stage and configured to deliver simultaneously respectively several sampled digital signals centered at the zero frequency and corresponding respectively to several selected channels.

3. (Original) The component according to Claim 1, wherein the channels extend over a predetermined frequency span and the analog signals convey digital information coded by digital modulation, and

wherein each channel decoding module comprises:

a decimator filter followed by an additional digital filter for eliminating information of adjacent channels; and

an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel being processed by the channel decoding module.

4. (Currently Amended) The component according to Claim 1, wherein the channels extend over a predetermined frequency span and the analog signals convey digital information coded by digital modulation, and

wherein the tuning module comprises:

an analog stage receiving the said analog signals;

a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the frequency span; and

several digital devices for transposing frequencies that are connected to the output of the analog conversion stage and configured to deliver simultaneously respectively several sampled digital signals centered at the zero frequency and corresponding respectively to several selected channels; and

wherein each channel decoding module comprises:

a decimator filter followed by an additional digital filter for eliminating information of adjacent channels; and

an error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel associated with the sampled digital signal processed by this channel decoding module.

5. (Original) The component according to Claim 4, wherein the resolution of the analog/digital conversion stage is greater than or equal to 6 bits.

6. (Original) The component according to Claim 4, wherein the decimator filter is a low-pass filter whose cutoff frequency is of the order of twice the frequency half-width of a channel, and wherein the cutoff frequency of the additional digital filter is of the order of the frequency half-width of a channel.

7. (Original) The component according to Claim 1, further comprising a grounding metal plate glued to a rear face of the substrate by a conducting glue.

8. (Original) The component according to Claim 1, wherein the substrate has a first type of conductivity and elements performing a digital processing are disposed in a part of the substrate that is insulated from the remaining part of the substrate by a semiconducting barrier having a second type of conductivity different from the first type of conductivity, and wherein the semiconducting barrier is biased by a bias voltage different from that used for the insulated part of the substrate.

9. (Original) The component of Claim 1, wherein the electronic component comprises a satellite digital television signal receiver.

10. (Previously Presented) An integrated circuit, comprising:

a monolithic substrate in which the following circuit components are provided:

an input receiving an analog signal including a plurality of channels;

an analog-to-digital converter to convert the analog signal to a digital signal;

a first digital tuner that downconverts the digital signal to a first downconverted digital signal, wherein information of a selected first channel in the downconverted digital signal is centered at zero frequency;

a first channel decoding digital module connected to the first digital tuner that decodes the first downconverted digital signal to output a stream of data packets for the selected first channel;

a second digital tuner that downconverts the digital signal to a second downconverted digital signal, wherein information of a selected second channel in the downconverted digital signal is centered at zero frequency; and

a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel.

11. (Original) The circuit of claim 10 wherein the first and second digital tuners are each of a direct sampling type which performs frequency transposition and channel selection in a digital domain.

12. (Original) The circuit of claim 10 wherein the analog-to-digital converter oversamples the received analog signal.

13. (Original) The circuit of claim 10 wherein the analog signal conveys information for the plurality of channels by digital modulation.

14. (Original) The circuit of claim 10 wherein the channels of the analog signal extend over a frequency span and wherein the analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the frequency span.

15. (Original) The circuit of claim 14 wherein the analog signal comprises a satellite digital television analog signal.

16. (Original) The circuit of claim 10 wherein each of the decoding digital modules comprises:

a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information;

a digital filter that filters out the adjacent channel information; and

an error correction stage to produce the data packets from the selected channel information.

17. (Original) The circuit of claim 16 wherein the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel.

18. (Original) The circuit of claim 17 wherein the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel.

19. (Original) The circuit of claim 10 further comprising a metal plate attached to a rear surface of the substrate.

20. (Original) The circuit of claim 10 wherein the integrated circuit is a component within a satellite digital television signal receiver.

21. (Previously Presented) An integrated circuit, comprising:

a monolithic substrate in which the following circuit components are provided:

an input receiving an analog signal including a plurality of channels;

a first analog-to-digital converter to convert the analog signal to a first digital signal;

a second analog-to-digital converter to convert the analog signal to a second digital signal;

a first digital tuner that downconverts a received digital signal to a first downconverted digital signal, wherein information of a selected first channel in the downconverted digital signal is centered at zero frequency;

a first channel decoding digital module connected to the first digital tuner that decodes the first downconverted digital signal to output a stream of data packets for the selected first channel;

a second digital tuner that downconverts a received digital signal to a second downconverted digital signal, wherein information of a selected second channel in the downconverted digital signal is centered at zero frequency;

a second channel decoding digital module connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel; and

a switching circuit that selectively couples the first and second digital signals to the first and second digital tuners.

22. (Original) The circuit of claim 21 wherein the first analog-to-digital converter is associated with analog signals in a first passband and wherein the second analog-to-digital converter is associated with analog signals in a second passband.

23. (Original) The circuit of claim 22 wherein, if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second digital tuners to the first analog-to-digital converter.

24. (Original) The circuit of claim 22 wherein, if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second digital tuners to the second analog-to-digital converter.

25. (Original) The circuit of claim 22 wherein, if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first digital tuner to the first analog-to-digital converter and the second digital tuner to the second analog-to-digital converter.

26. (Original) The circuit of claim 22 wherein, if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first digital tuner to the second analog-to-digital converter and the second digital tuner to the first analog-to-digital converter.

27. (Original) The circuit of claim 22 further including:

a first filter tuned to the first passband that outputs the analog signal to the first analog-to-digital converter; and

a second filter tuned to the second passband that outputs the analog signal to the second analog-to-digital converter.

28. (Original) The circuit of claim 21 wherein the first and second digital tuners are each of a direct sampling type which performs frequency transposition and channel selection in a digital domain.

29. (Original) The circuit of claim 21 wherein each analog-to-digital converter oversamples the received analog signal.

30. (Original) The circuit of claim 21 wherein the analog signal conveys information for the plurality of channels by digital modulation.

31. (Original) The circuit of claim 21 wherein the channels of the analog signal applied to each analog-to-digital converter extend over a given frequency span and wherein each analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the given frequency span.

32. (Original) The circuit of claim 31 wherein the analog signal comprises a satellite digital television analog signal.

33. (Original) The circuit of claim 21 wherein each of the decoding digital modules comprises:

a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information;

a digital filter that filters out the adjacent channel information; and

an error correction stage to produce the data packets from the selected channel information.

34. (Original) The circuit of claim 33 wherein the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel.

35. (Original) The circuit of claim 34 wherein the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel.

36. (Original) The circuit of claim 21 further comprising a metal plate attached to a rear surface of the substrate.

37. (Original) The circuit of claim 21 wherein the integrated circuit is a component within a satellite digital television signal receiver.

38. (Original) An electronic device, comprising:

an integrated circuit embodied on a monolithic substrate and incorporating:

a multi-channel direct sampling type tuner that receives an analog signal composed of several channels and outputs first and second channel digital signals;

a first channel decoder that receives the first channel digital signal and outputs a first channel stream of data packets; and

a second channel decoder that receives the second channel digital signal and outputs a second channel stream of data packets.

39. (Original) The device of claim 38 wherein the multi-channel direct sampling type tuner comprises:

at least one analog-to-digital converter to convert the received analog signal to a digital signal;

a first frequency transposition circuit that downconverts the digital signal to the first channel digital signal; and

a second frequency transposition circuit that downconverts the digital signal to the second channel digital signal.

40. (Original) The device of claim 39 wherein the multi-channel direct sampling type tuner comprises a first and second analog-to-digital converter that convert the received analog signal to a first and second digital signal, and a switching circuit that selectively couples the first and second digital signals to the first and second frequency transposition circuits.

41. (Original) The circuit of claim 40 wherein the first analog-to-digital converter is associated with analog signals in a first passband and wherein the second analog-to-digital converter is associated with analog signals in a second passband.

42. (Original) The circuit of claim 41 wherein, if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second frequency transposition circuits to the first analog-to-digital converter.

43. (Original) The circuit of claim 41 wherein, if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second frequency transposition circuits to the second analog-to-digital converter.

44. (Original) The circuit of claim 41 wherein, if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first frequency transposition circuit to the first analog-to-digital converter and the second frequency transposition circuit to the second analog-to-digital converter.

45. (Original) The circuit of claim 41 wherein, if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first frequency transposition circuit to the second analog-to-digital converter and the second frequency transposition circuit to the first analog-to-digital converter.

46. (Original) The circuit of claim 41 further including:

a first filter tuned to the first passband that outputs the analog signal to the first analog-to-digital converter; and

a second filter tuned to the second passband that outputs the analog signal to the second analog-to-digital converter.

47. (Original) The circuit of claim 38 wherein the analog-to-digital converter oversamples the received analog signal.

48. (Original) The circuit of claim 38 wherein the analog signal conveys information for the plurality of channels by digital modulation.

49. (Original) The circuit of claim 38 wherein the channels of the analog signal extend over a frequency span and wherein the analog-to-digital converter oversamples the received analog signal at a sampling frequency at least twice the frequency span.

50. (Original) The circuit of claim 49 wherein the analog signal comprises a satellite digital television analog signal.

51. (Original) The circuit of claim 38 wherein each of the channel decoder comprises:

a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information;

a digital filter that filters out the adjacent channel information; and

an error correction stage to produce the data packets from the selected channel information.

52. (Original) The circuit of claim 51 wherein the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel.

53. (Original) The circuit of claim 52 wherein the digital filter is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel.

54. (Original) The circuit of claim 38 further comprising a metal plate attached to a rear surface of the substrate.

55. (Original) The circuit of claim 38 wherein the integrated circuit is a component within a satellite digital television signal receiver.